

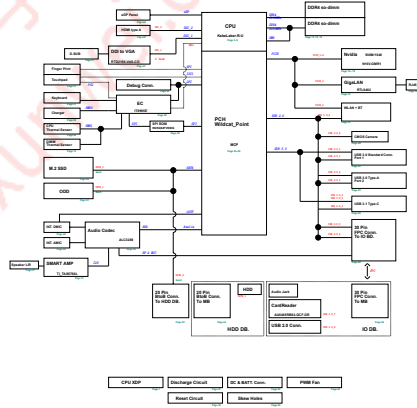
PCB POWER PLANE MAP

PCB POWER PLANE MAP
1. CPU Power Plane
2. GPU Power Plane
3. Memory Power Plane
4. Storage Power Plane
5. Peripheral Power Plane
6. System Power Plane
7. USB Power Plane
8. Ethernet Power Plane
9. SATA Power Plane
10. Display Power Plane
11. Audio Power Plane
12. Fan Power Plane
13. LED Power Plane
14. Miscellaneous Power Plane
15. Ground Plane
16. Power Plane Summary
17. Power Plane Legend
18. Power Plane Notes
19. Power Plane Revision History
20. Power Plane Contact Information

# X542UN/URV SCHEMATIC Revision 1.0

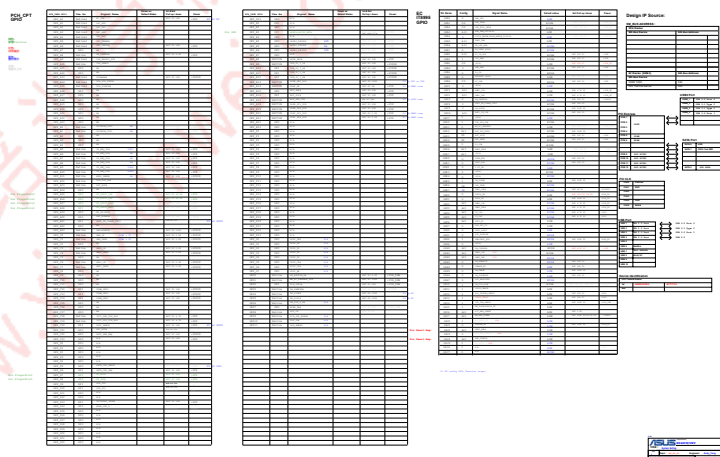
( N16 : DGPU = Nvidia N16S-GMR, 512MB )  
( N17 : DGPU = Nvidia N17S-G1, 512MB )

Non Connected Standby



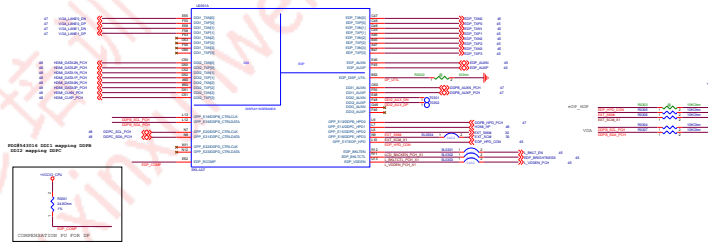
## BLOCK DIAGRAM



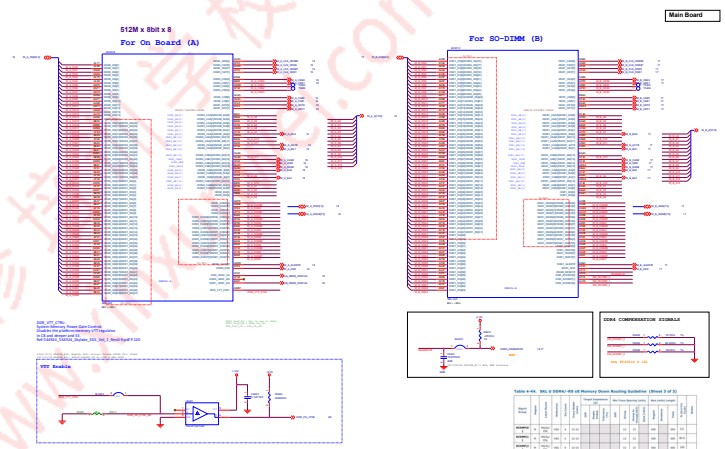


Main Board

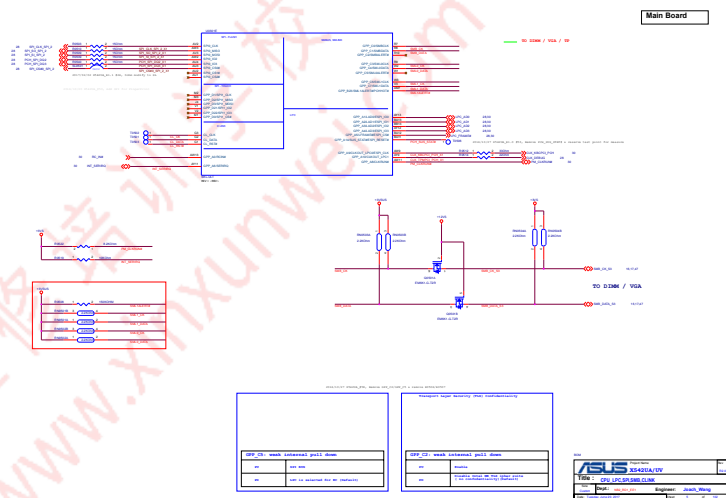
Display Port	Intel Version	ASUS P/N
A	BDP	
B	BDP	
C	BDP	



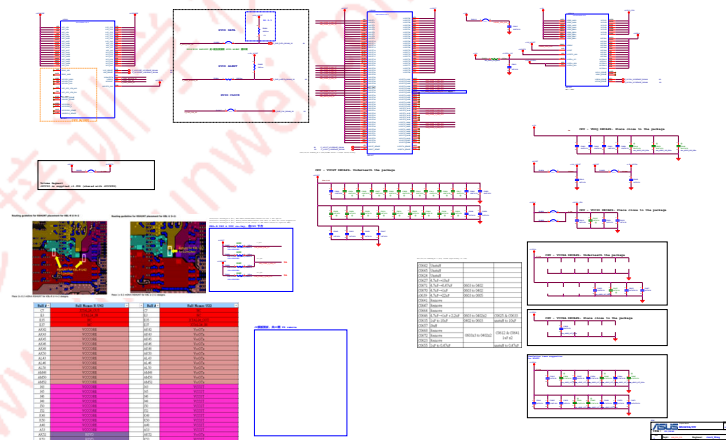
ASUS		20420A/0Y	
File	20420A/0Y	Engineer	chuck.ning
Rev	1.0	Date	2011.01.01



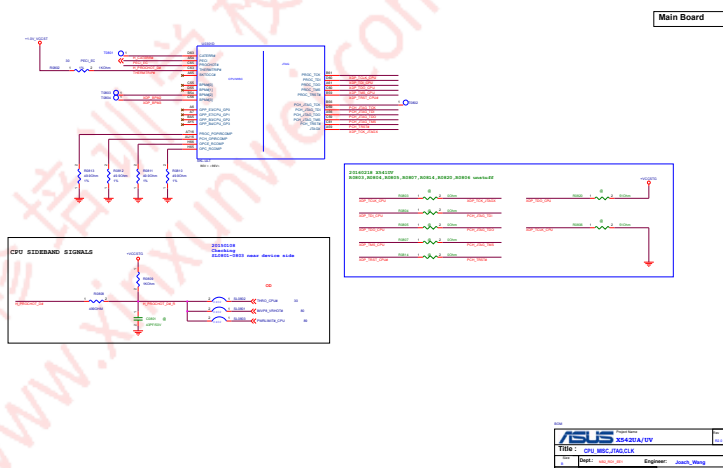




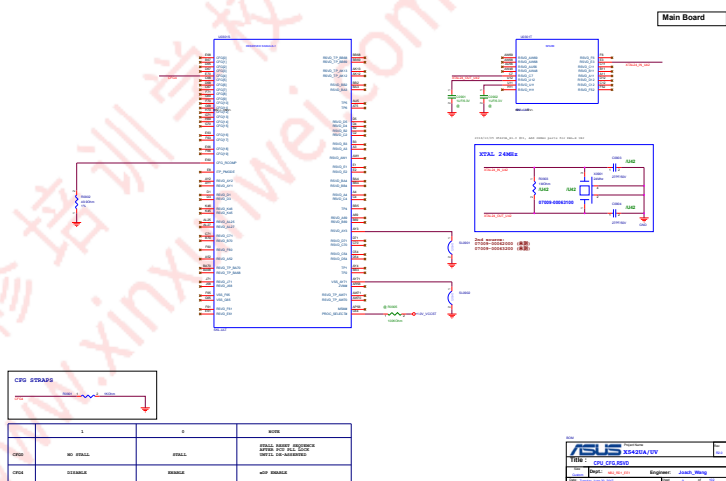
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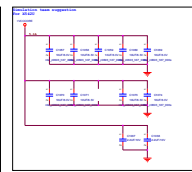
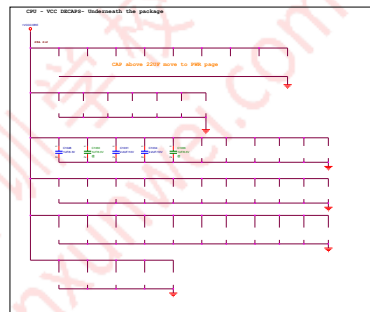
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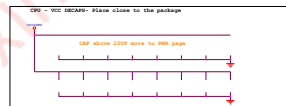
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C1072	Remove		
C1037	Add	add 0402	2.2uF
C1038	Add	add 0402	2.2uF
C1031	1uF to 2.2uF		unstuff to 2.2uF
C1034	1uF to 2.2uF		unstuff to 2.2uF

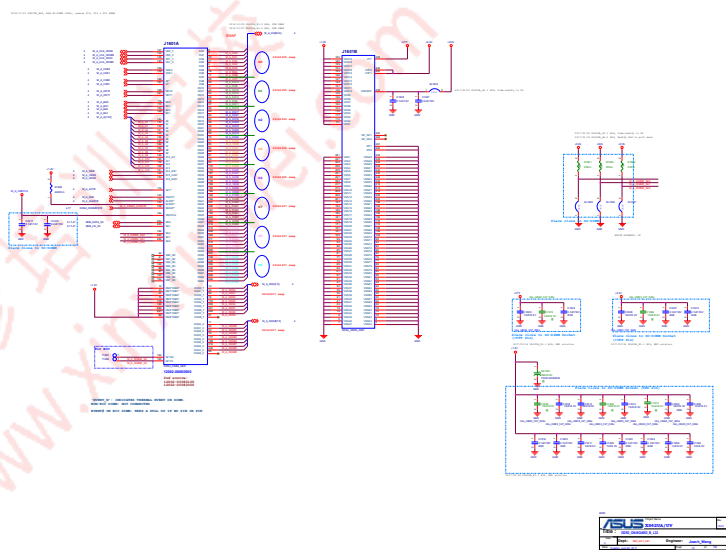


~~Not for Distribution~~

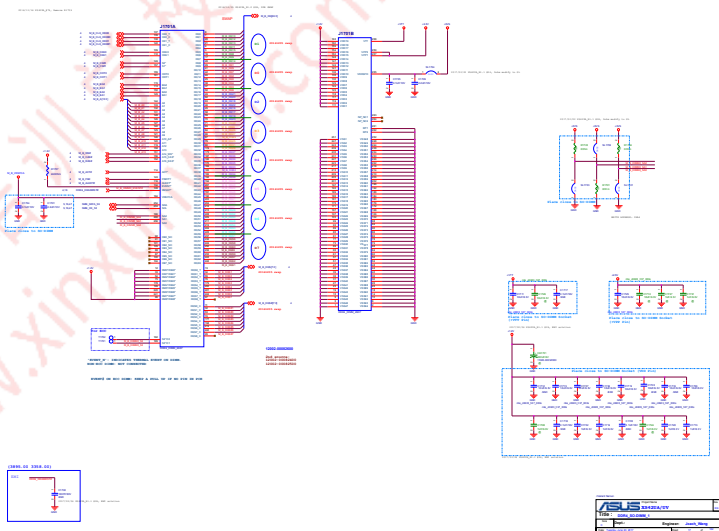
9.27

SAL Processor and Memory Type	SAL N				
	D0M4-AS N0 D0M4-EE	D0M4-AS N0 D0M4-EE	D0M4-AS N0 D0M4-EE	D0M4-AS N0 D0M4-EE	L0D0S Memory Stream
<b>Signal Group Details</b>					
Clear (CLK)	CN0[3:0], CNP[3:0]	CN0[3:0], CNP[3:0]	CN0[3:0], CNP[3:0]	CN0[3:0], CNP[3:0]	CN0[3:0], CN0C[3:0]
Clear (EN)	CN0[3:0], CNP[3:0]	CN0[3:0], CNP[3:0]	CN0[3:0], CNP[3:0]	CN0[3:0], CNP[3:0]	CN0[3:0], CN0C[3:0]
Clear (done)	CN0[3:0], CNP[3:0]	CN0[3:0], CNP[3:0]	CN0[3:0], CNP[3:0]	CN0[3:0], CNP[3:0]	CN0[3:0], CN0C[3:0]
Command (CMD)	MCN[3:0], B0E[3:0] B0C[3:0], B0E[3:0]	MCN[3:0], B0E[3:0] B0C[3:0], B0E[3:0]	MCN[3:0], B0E[3:0] B0C[3:0], B0E[3:0]	MCN[3:0], B0E[3:0] B0C[3:0], B0E[3:0]	CAN[3:0], CAN0C[3:0]
Stroke	D0M7[3:0] D0M7C[3:0]	D0M7[3:0] D0M7C[3:0]	D0M7[3:0] D0M7C[3:0]	D0M7[3:0] D0M7C[3:0]	D0M7[3:0] D0M7C[3:0]
ENL stroke	N/A	N/A	N/A	N/A	N/A
ENL	D0M7C[3:0]	D0M7C[3:0]	D0M7C[3:0]	D0M7C[3:0]	D0M7C[3:0]
ENL data	D0M7C[3:0]	D0M7C[3:0]	D0M7C[3:0]	D0M7C[3:0]	D0M7C[3:0]
ENL data	D0M7C[3:0]	N/A	N/A	N/A	N/A
Alert	ALERT[3:0]	ALERT[3:0]	ALERT[3:0]	ALERT[3:0]	N/A
Alert	ALERT[3:0]	ALERT[3:0]	ALERT[3:0]	ALERT[3:0]	N/A
RCOMP	D0R_RCOMP[0:1]	D0R_RCOMP[0:1]	D0R_RCOMP[0:1]	D0R_RCOMP[0:1]	D0R_RCOMP[0:1]





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Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down V<sub>REF-CA</sub> Overview

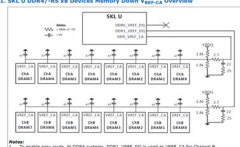
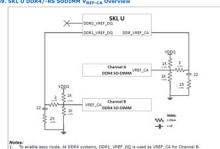
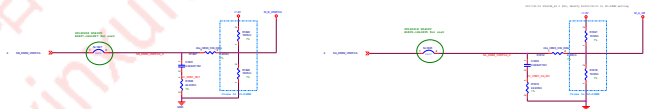
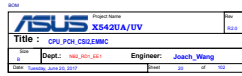


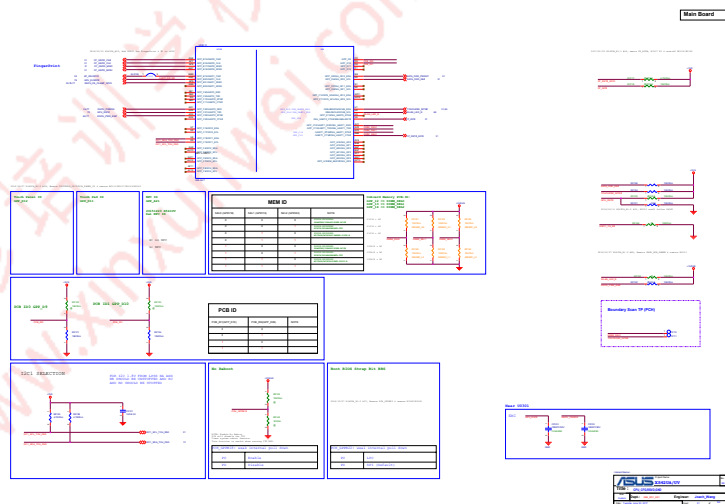
Figure 4-49. SKL U DDR4/-RS SODIMM V<sub>DDQ-CA</sub> Overview



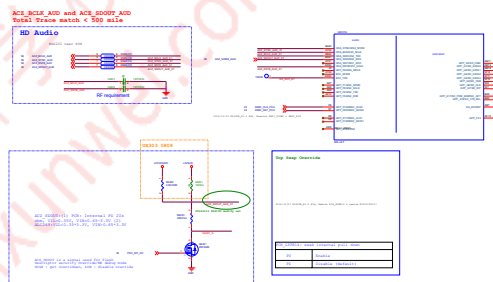
All Vref trace must be 20 mils width



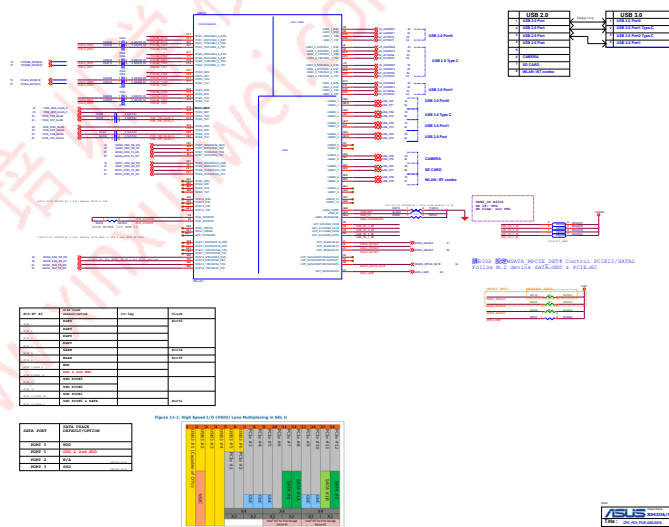




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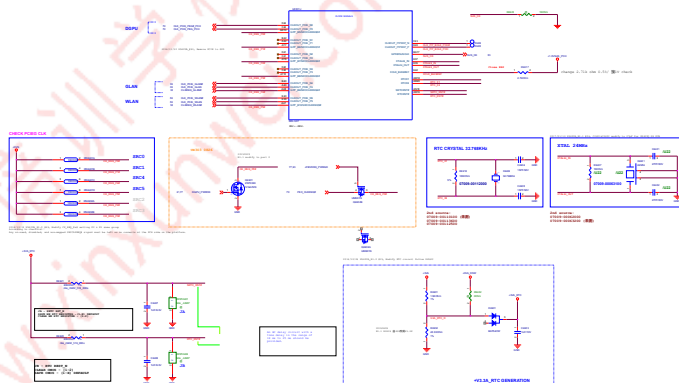


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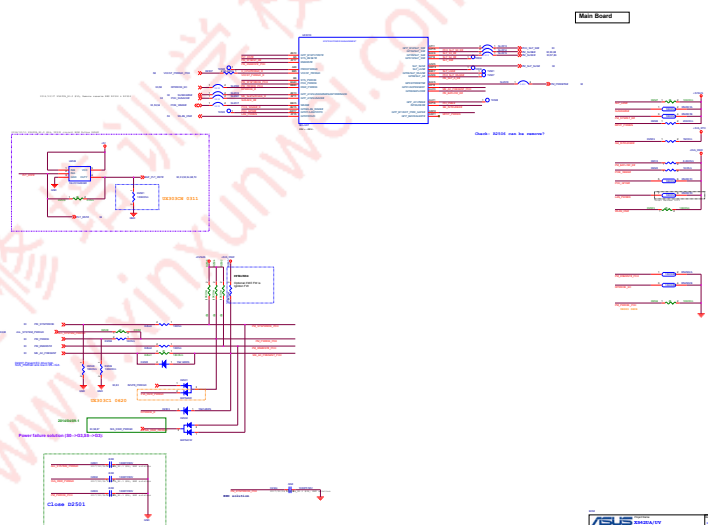
		Motherboard <b>X38D30A/EV</b>	
P2B0 :		GPU: PCI:PCRAM:GATA	
Date:	Dept.:	Engineer:	Joseph Wang

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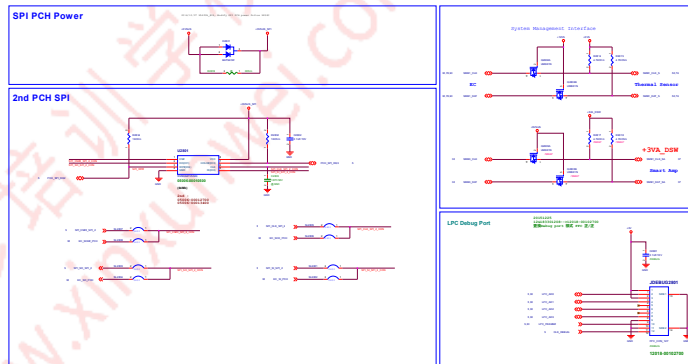


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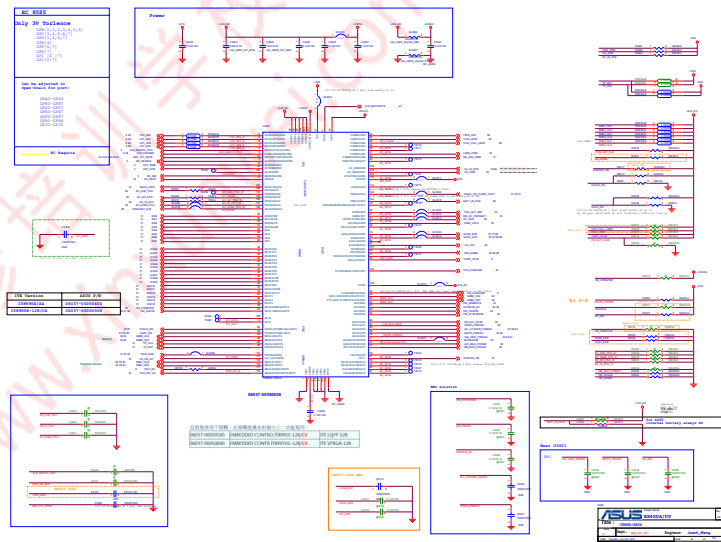








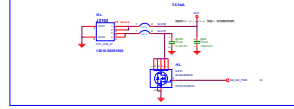




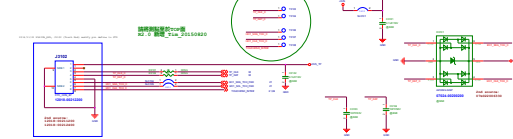
Internal Keyboard



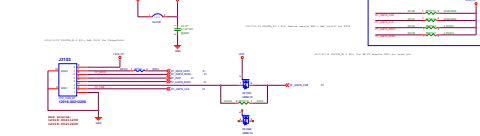
KB BL CON



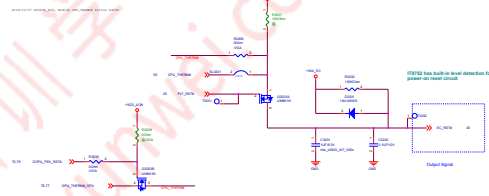
Touch PAD



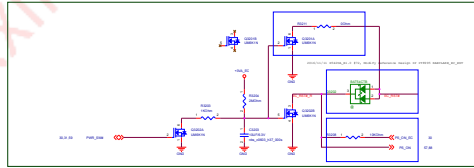
Fingerprint



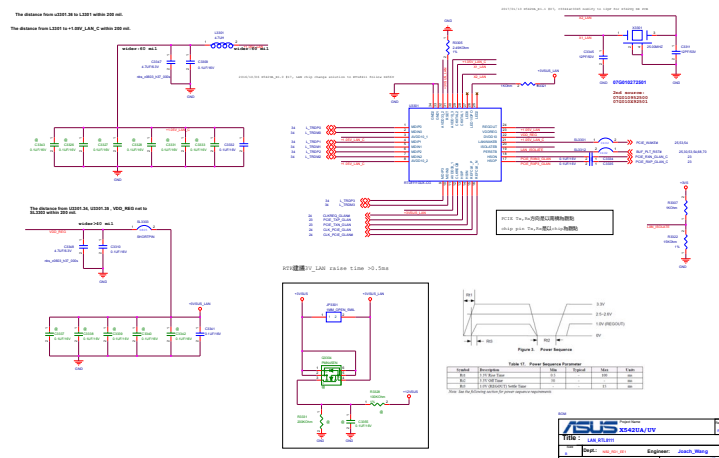
### Thermal Policy



battery embedded (press pwr\_sw 10sec, then reset ec)

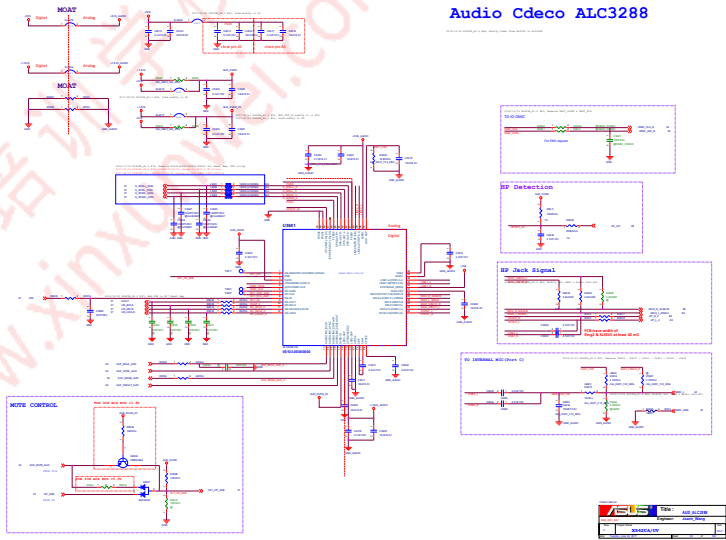


ASUS	
Model	ASUS
Part	ASUS
Rev	ASUS
Rev	ASUS









Audio Cdeco ALC3288

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# SMART AMP. & SPK

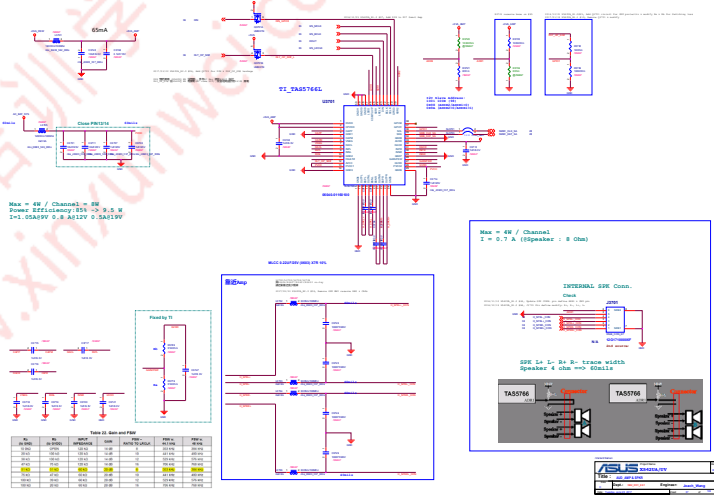
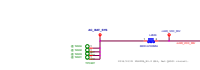
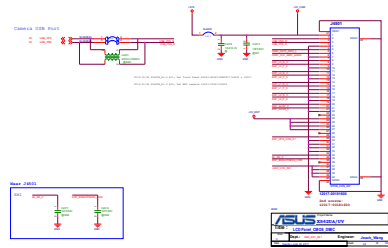
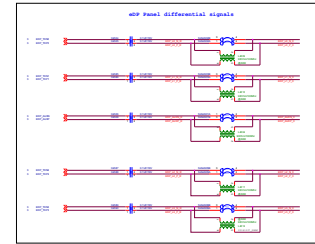
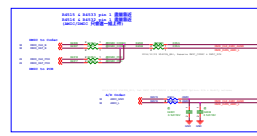


Table 1: Component values for the proposed converter.

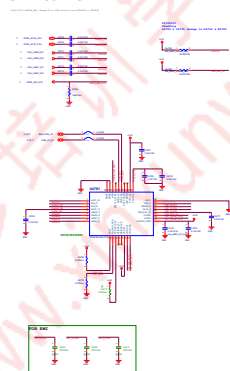
Component	Value	Unit
$L_r$	100	$\mu H$
$C_r$	1000	$nF$
$L_p$	100	$\mu H$
$L_s$	100	$\mu H$
$C_f$	1000	$nF$
$R_{ds(on)}$	0.01	$\Omega$
$R_{cr}$	0.01	$\Omega$
$R_{ls}$	0.01	$\Omega$
$R_{ld}$	10	$\Omega$
$R_{cr}$	10	$\Omega$
$R_{ld}$	10	$\Omega$
$R_{cr}$	10	$\Omega$
$R_{ld}$	10	$\Omega$
$R_{cr}$	10	$\Omega$



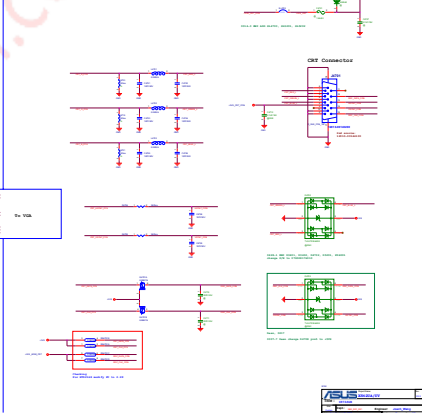
The diagram illustrates the lac operon. At the top, the DNA sequence is shown with the *lacZ* gene, *lacY* gene, and *lacA* gene. The *lacO* (operator) site is located between the *lacP* (promoter) and the structural genes. A repressor protein, labeled "REPRESSOR PROTEIN" and "binds to the operator", is shown bound to the *lacO* site. This binding prevents RNA polymerase from transcribing the structural genes. The *lacP* site is also labeled. The *lacZ* gene is transcribed into mRNA, which is then translated into a protein. The *lacY* gene is also transcribed into mRNA, which is then translated into a protein. The *lacA* gene is transcribed into mRNA, which is then translated into a protein.



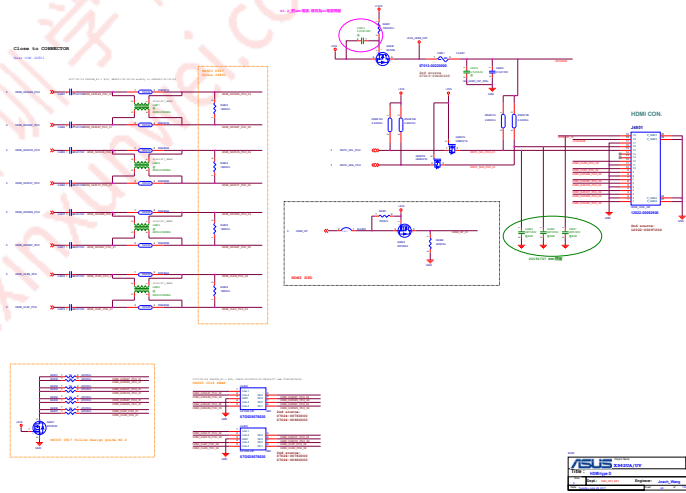
### eDP to VGA



### CRT D-SUB



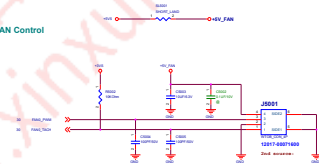
## HDMI type-A



### CPU Thermal Sensor



### DC FAN Control



請將測試點於CPU面  
3.2.0 設置 \*Pin\_01150820

### 5.3 Address Setting

NCT7715U I2C Slave address is 1010001b (x is RW bit).

### 5.6 ALERT# point hardware power-on setting (TBD)

The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin.

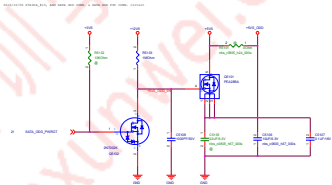
PULL-UP RESISTOR	TEMPERATURE (°C)
2KΩ	75
7.5KΩ	90
10.5KΩ	100
1.6KΩ	105
16.7KΩ	110

Route CPU\_THERM\_0A, CPU\_THERM\_0C and on the same layer.

10 mils — OTHER SIGNALS  
10 mils — CPU\_THERM\_0A  
10 mils — CPU\_THERM\_0C  
10 mils — CPU\_THERM\_0E  
10 mils — CPU\_THERM\_0F  
10 mils — CPU\_THERM\_0G  
10 mils — CPU\_THERM\_0H  
10 mils — CPU\_THERM\_0I  
10 mils — CPU\_THERM\_0J  
10 mils — CPU\_THERM\_0K  
10 mils — CPU\_THERM\_0L  
10 mils — CPU\_THERM\_0M  
10 mils — CPU\_THERM\_0N  
10 mils — CPU\_THERM\_0O  
10 mils — CPU\_THERM\_0P  
10 mils — CPU\_THERM\_0Q  
10 mils — CPU\_THERM\_0R  
10 mils — CPU\_THERM\_0S  
10 mils — CPU\_THERM\_0T  
10 mils — CPU\_THERM\_0U  
10 mils — CPU\_THERM\_0V  
10 mils — CPU\_THERM\_0W  
10 mils — CPU\_THERM\_0X  
10 mils — CPU\_THERM\_0Y  
10 mils — CPU\_THERM\_0Z



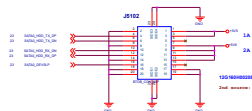
### SATA ODD CONN.



This schematic diagram illustrates the wiring for a SATA ODD (Optical Drive) connector. It shows a 15-pin connector with the following connections:

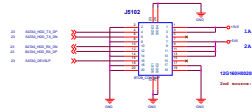
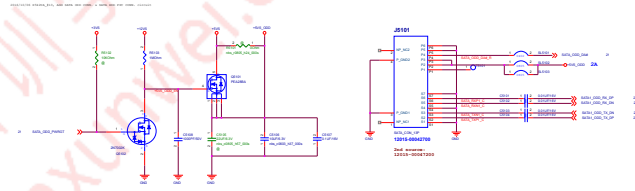
- Pin 1 (SATA\_0001\_P000001) to Pin 15 (SATA\_0001\_P000015) via a 10kΩ resistor.
- Pin 2 (SATA\_0001\_P000002) to Pin 14 (SATA\_0001\_P000014) via a 10kΩ resistor.
- Pin 3 (SATA\_0001\_P000003) to Pin 13 (SATA\_0001\_P000013) via a 10kΩ resistor.
- Pin 4 (SATA\_0001\_P000004) to Pin 12 (SATA\_0001\_P000012) via a 10kΩ resistor.
- Pin 5 (SATA\_0001\_P000005) to Pin 11 (SATA\_0001\_P000011) via a 10kΩ resistor.
- Pin 6 (SATA\_0001\_P000006) to Pin 10 (SATA\_0001\_P000010) via a 10kΩ resistor.
- Pin 7 (SATA\_0001\_P000007) to Pin 9 (SATA\_0001\_P000009) via a 10kΩ resistor.
- Pin 8 (SATA\_0001\_P000008) to Pin 8 (SATA\_0001\_P000008) via a 10kΩ resistor.
- Pin 9 (SATA\_0001\_P000009) to Pin 7 (SATA\_0001\_P000007) via a 10kΩ resistor.
- Pin 10 (SATA\_0001\_P000010) to Pin 6 (SATA\_0001\_P000006) via a 10kΩ resistor.
- Pin 11 (SATA\_0001\_P000011) to Pin 5 (SATA\_0001\_P000005) via a 10kΩ resistor.
- Pin 12 (SATA\_0001\_P000012) to Pin 4 (SATA\_0001\_P000004) via a 10kΩ resistor.
- Pin 13 (SATA\_0001\_P000013) to Pin 3 (SATA\_0001\_P000003) via a 10kΩ resistor.
- Pin 14 (SATA\_0001\_P000014) to Pin 2 (SATA\_0001\_P000002) via a 10kΩ resistor.
- Pin 15 (SATA\_0001\_P000015) to Pin 1 (SATA\_0001\_P000001) via a 10kΩ resistor.

### SATA HDD BtoB CONN.

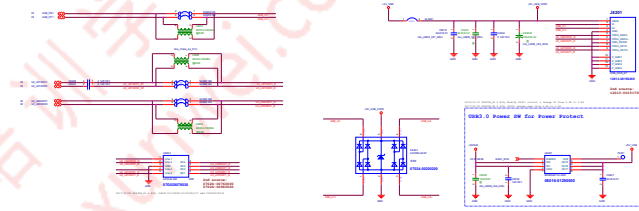


This schematic diagram illustrates the wiring for a SATA HDD BtoB (Back-to-Back) connector. It shows a 15-pin connector with the following connections:

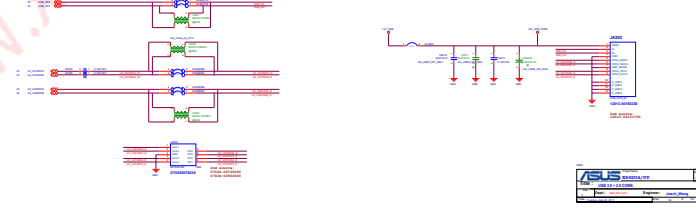
- Pin 1 (SATA\_0001\_P000001) to Pin 15 (SATA\_0001\_P000015) via a 10kΩ resistor.
- Pin 2 (SATA\_0001\_P000002) to Pin 14 (SATA\_0001\_P000014) via a 10kΩ resistor.
- Pin 3 (SATA\_0001\_P000003) to Pin 13 (SATA\_0001\_P000013) via a 10kΩ resistor.
- Pin 4 (SATA\_0001\_P000004) to Pin 12 (SATA\_0001\_P000012) via a 10kΩ resistor.
- Pin 5 (SATA\_0001\_P000005) to Pin 11 (SATA\_0001\_P000011) via a 10kΩ resistor.
- Pin 6 (SATA\_0001\_P000006) to Pin 10 (SATA\_0001\_P000010) via a 10kΩ resistor.
- Pin 7 (SATA\_0001\_P000007) to Pin 9 (SATA\_0001\_P000009) via a 10kΩ resistor.
- Pin 8 (SATA\_0001\_P000008) to Pin 8 (SATA\_0001\_P000008) via a 10kΩ resistor.
- Pin 9 (SATA\_0001\_P000009) to Pin 7 (SATA\_0001\_P000007) via a 10kΩ resistor.
- Pin 10 (SATA\_0001\_P000010) to Pin 6 (SATA\_0001\_P000006) via a 10kΩ resistor.
- Pin 11 (SATA\_0001\_P000011) to Pin 5 (SATA\_0001\_P000005) via a 10kΩ resistor.
- Pin 12 (SATA\_0001\_P000012) to Pin 4 (SATA\_0001\_P000004) via a 10kΩ resistor.
- Pin 13 (SATA\_0001\_P000013) to Pin 3 (SATA\_0001\_P000003) via a 10kΩ resistor.
- Pin 14 (SATA\_0001\_P000014) to Pin 2 (SATA\_0001\_P000002) via a 10kΩ resistor.
- Pin 15 (SATA\_0001\_P000015) to Pin 1 (SATA\_0001\_P000001) via a 10kΩ resistor.



USB3.0\_Port 0

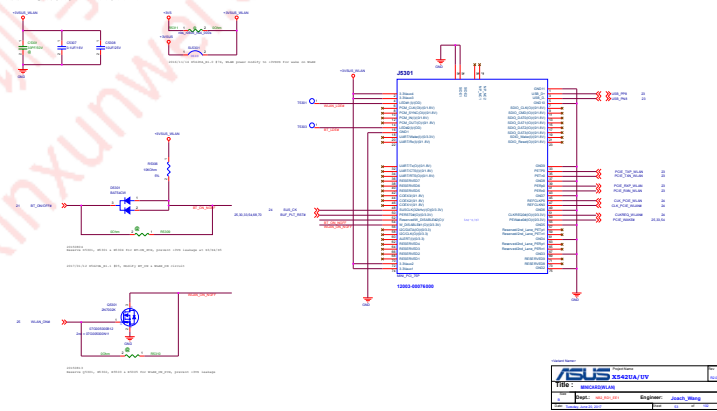


USB3.0\_Port 1

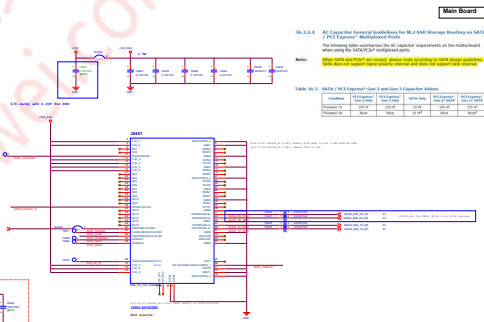




## WLAN CONN.



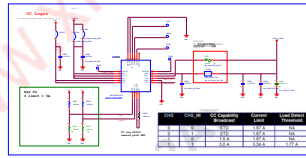
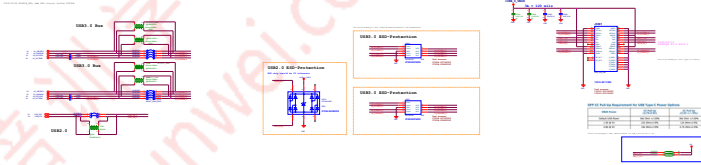
2016/01/06 01:29:56, add new domain follow 000000

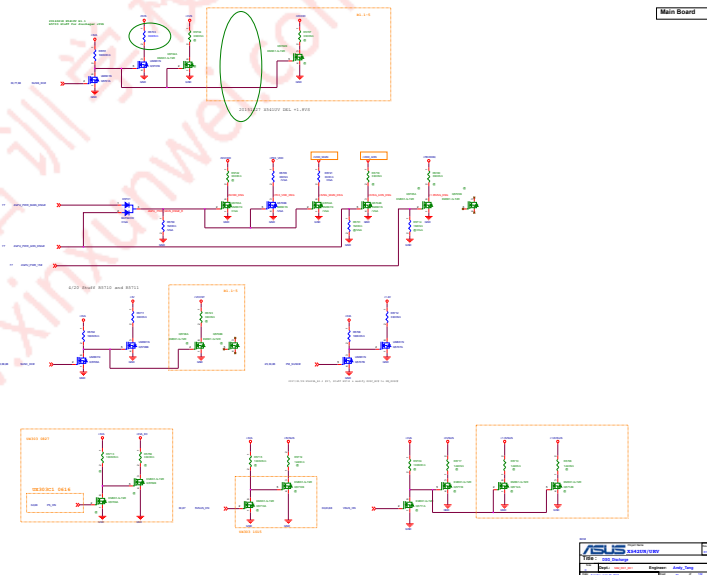


Condition	PCI Express® Gen 2 Only	PCI Express® Gen 3 Only	SATA Only	PCI Express® Gen 2 / SATA	PCI Express® Gen 3 / SATA
Acoustic Pa	100 uF	100 uF	100 uF	100 uF	100 uF
Acoustic Pa	None	None	10 uF	None	None

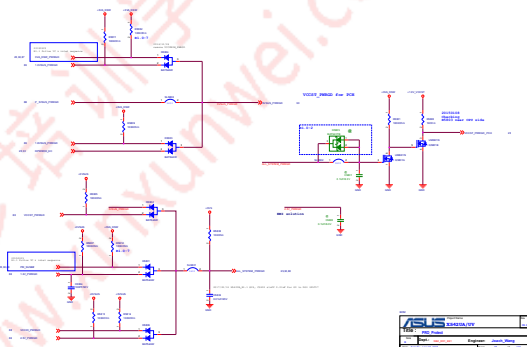


# USB 3.0 TypeC CONN.



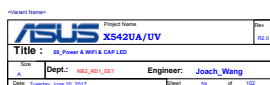


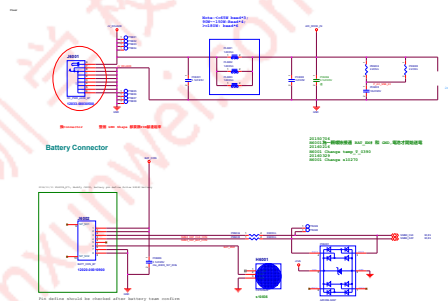
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Main Board

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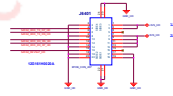


4-pin connector pin define  
(請參見圖)

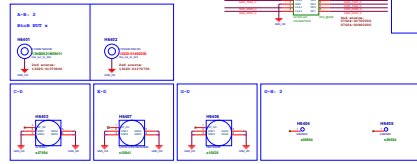
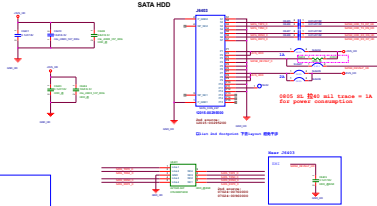
Pin	Signal	Description	Remark
1	P+	Battery pack positive terminal	Inductor voltage
2	P-	Battery pack negative terminal	Inductor voltage
3	SMBC	Serial clock input	SMBC
4	SMDS	Serial data input	SMBC
5	NC	Not connected	
6	ENH	Battery pack enable input	SMBC
7	P+	Battery pack positive terminal	SMBC
8	P-	Battery pack negative terminal	SMBC



### SATA HDD BtoB CONN.



### SATA HDD CONN.



Pin	Signal	Color
1	NC	
2	NC	
3	NC	
4	NC	
5	NC	
6	NC	
7	NC	
8	NC	
9	NC	
10	NC	
11	NC	
12	NC	
13	NC	
14	NC	
15	NC	
16	NC	
17	NC	
18	NC	
19	NC	
20	NC	
21	NC	
22	NC	
23	NC	
24	NC	
25	NC	
26	NC	
27	NC	
28	NC	
29	NC	
30	NC	
31	NC	
32	NC	
33	NC	
34	NC	
35	NC	
36	NC	
37	NC	
38	NC	
39	NC	
40	NC	
41	NC	
42	NC	
43	NC	
44	NC	
45	NC	
46	NC	
47	NC	
48	NC	
49	NC	
50	NC	
51	NC	
52	NC	
53	NC	
54	NC	
55	NC	
56	NC	
57	NC	
58	NC	
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68	NC	
69	NC	
70	NC	
71	NC	
72	NC	
73	NC	
74	NC	
75	NC	
76	NC	
77	NC	
78	NC	
79	NC	
80	NC	
81	NC	
82	NC	
83	NC	
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85	NC	
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87	NC	
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89	NC	
90	NC	
91	NC	
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93	NC	
94	NC	
95	NC	
96	NC	
97	NC	
98	NC	
99	NC	
100	NC	

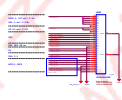




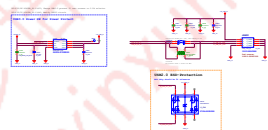
#### DB\_IO

DB\_IO

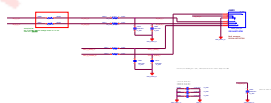
#### HDD DB to IO DB FPC CONN.



#### USB 2.0 con.

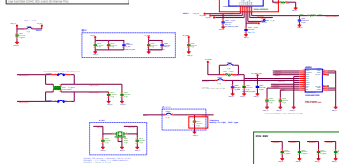


#### AUDIO JACK



#### SD Card Reader

Pin	Signal	Color
1	VCC	Red
2	IO	Green
3	GND	Black
4	IO	Green
5	VCC	Red
6	GND	Black
7	IO	Green
8	VCC	Red
9	GND	Black
10	IO	Green
11	VCC	Red
12	GND	Black
13	IO	Green
14	VCC	Red
15	GND	Black

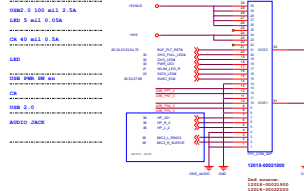
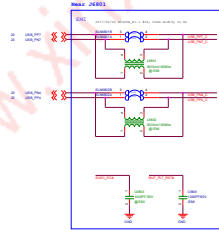


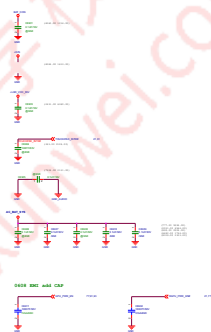
#### LED indicator

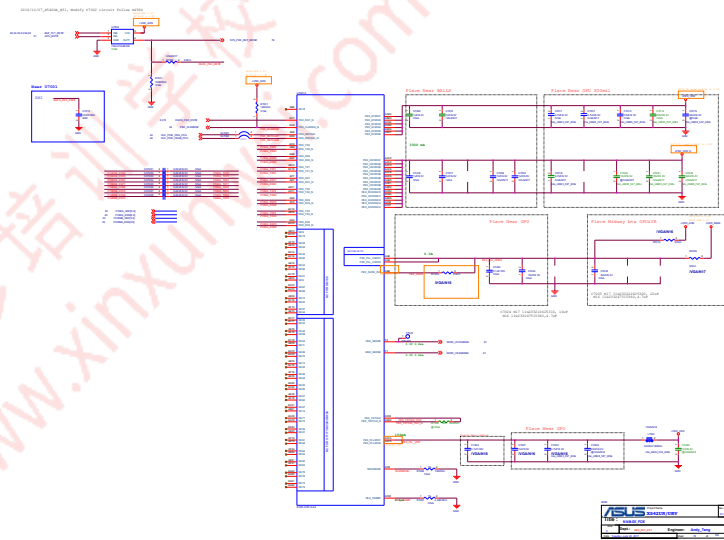


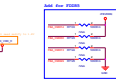
MB to Board to IO FPC CONN.

MB to IO DB FPC CONN.









GM2-4, GM3-4, GM4-13	Channel 0 3_31	GM3-4, GM3-4A, GM4-13	Channel 1 32_4
CM00	C5*	CM07	C5*
CM01	A1, S43	CM17	A1, S43
CM02	D2, S40	CM18	D2, S40
CM03	A4, S42	CM19	A4, S42
CM04	A5, S41	CM20	A5, S41
CM05	VR*	CM21	VR*
CM06	A7, A8	CM22	A7, A8
CM07	AB, A11	CM23	AB, A11
CM08	A9*	CM24	A9*
CM09	A12, SPU	CM25	A12, SPU
CM10	AB, A10	CM26	AB, A10
CM11	A1, A9	CM27	A1, A9
CM12	B4*	CM28	B4*
CM13	CR*	CM29	CR*
CM14	CR*	CM30	CR*
CM15	C4*	CM31	C4*

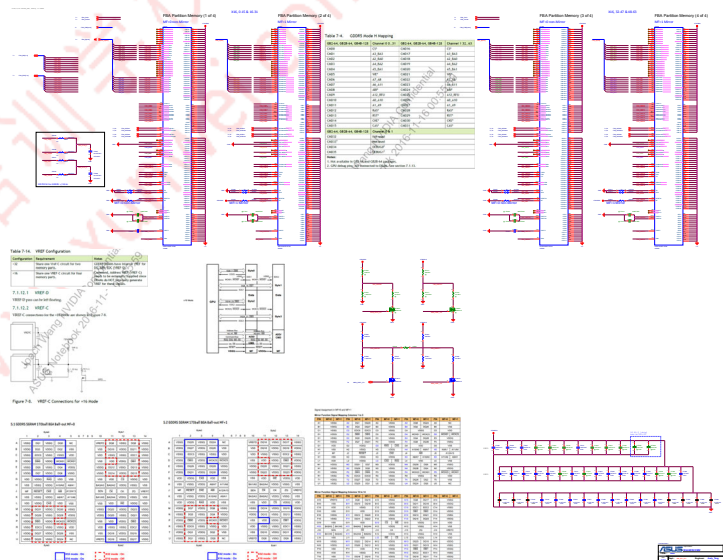
G82-64, G82B-64, G84B-128	Channel 0 & 1
CMD32	Hot used
CMD33 <sup>1</sup>	Hot used
CMD34	DEBUG <sup>2</sup>
CMD35	DEBUG <sup>1</sup>

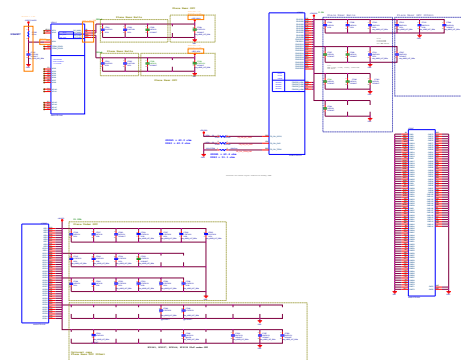
Notes:

1. Not available in G82-64 and G82B-64 packages.
2. GPU debug miss; not connected to DRAM. See section 7.1.13.

2. GPU debug pins not connected to GDM. See section 7.1.13.



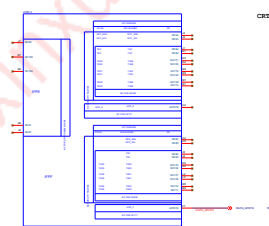
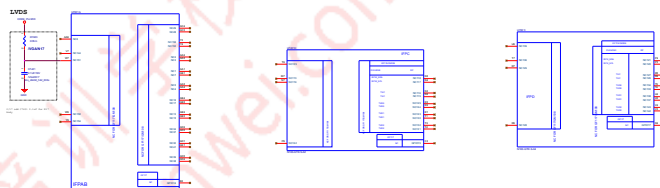




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40s

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[illegible]

Number Value	Push-Up to 10%_Push	Push-Up to 10%_Push
0.000	0.000	0.000
0.001	0.001	0.001
0.002	0.002	0.002
0.003	0.003	0.003
0.004	0.004	0.004
0.005	0.005	0.005
0.006	0.006	0.006
0.007	0.007	0.007
0.008	0.008	0.008
0.009	0.009	0.009
0.010	0.010	0.010
0.011	0.011	0.011
0.012	0.012	0.012
0.013	0.013	0.013
0.014	0.014	0.014
0.015	0.015	0.015
0.016	0.016	0.016
0.017	0.017	0.017
0.018	0.018	0.018
0.019	0.019	0.019
0.020	0.020	0.020
0.021	0.021	0.021
0.022	0.022	0.022
0.023	0.023	0.023
0.024	0.024	0.024
0.025	0.025	0.025
0.026	0.026	0.026
0.027	0.027	0.027
0.028	0.028	0.028
0.029	0.029	0.029
0.030	0.030	0.030
0.031	0.031	0.031
0.032	0.032	0.032
0.033	0.033	0.033
0.034	0.034	0.034
0.035	0.035	0.035
0.036	0.036	0.036
0.037	0.037	0.037
0.038	0.038	0.038
0.039	0.039	0.039
0.040	0.040	0.040
0.041	0.041	0.041
0.042	0.042	0.042
0.043	0.043	0.043
0.044	0.044	0.044
0.045	0.045	0.045
0.046	0.046	0.046
0.047	0.047	0.047
0.048	0.048	0.048
0.049	0.049	0.049
0.050	0.050	0.050
0.051	0.051	0.051
0.052	0.052	0.052
0.053	0.053	0.053
0.054	0.054	0.054
0.055	0.055	0.055
0.056	0.056	0.056
0.057	0.057	0.057
0.058	0.058	0.058
0.059	0.059	0.059
0.060	0.060	0.060
0.061	0.061	0.061
0.062	0.062	0.062
0.063	0.063	0.063
0.064	0.064	0.064
0.065	0.065	0.065
0.066	0.066	0.066
0.067	0.067	0.067
0.068	0.068	0.068
0.069	0.069	0.069
0.070	0.070	0.070
0.071	0.071	0.071
0.072	0.072	0.072
0.073	0.073	0.073
0.074	0.074	0.074
0.075	0.075	0.075
0.076	0.076	0.076
0.077	0.077	0.077
0.078	0.078	0.078
0.079	0.079	0.079
0.080	0.080	0.080
0.081	0.081	0.081
0.082	0.082	0.082
0.083	0.083	0.083
0.084	0.084	0.084
0.085	0.085	0.085
0.086	0.086	0.086
0.087	0.087	0.087
0.088	0.088	0.088
0.089	0.089	0.089
0.090	0.090	0.090
0.091	0.091	0.091
0.092	0.092	0.092
0.093	0.093	0.093
0.094	0.094	0.094
0.095	0.095	0.095
0.096	0.096	0.096
0.097	0.097	0.097
0.098	0.098	0.098
0.099	0.099	0.099
0.100		

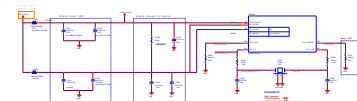
[illegible]

Strip No	Strip Configuration No	Comment
Strip_1	AWT_000000(1-1)	Full size unsplit and use 14 samples
Strip_21		
Strip_22		
Strip_23		
Strip_24	AWT_000000(1-1)	
Strip_25	AWT_000000(1-1)	
Strip_26	AWT_000000(1-1)	
Strip_27	AWT_000000(1-1)	
Strip_28	AWT_000000(1-1)	
Strip_29	AWT_000000(1-1)	
Strip_30	AWT_000000(1-1)	
Strip_31	AWT_000000(1-1)	
Strip_32	AWT_000000(1-1)	
Strip_33	AWT_000000(1-1)	
Strip_34	AWT_000000(1-1)	
Strip_35	AWT_000000(1-1)	
Strip_36	AWT_000000(1-1)	
Strip_37	AWT_000000(1-1)	
Strip_38	AWT_000000(1-1)	
Strip_39	AWT_000000(1-1)	
Strip_40	AWT_000000(1-1)	
Strip_41	AWT_000000(1-1)	
Strip_42	AWT_000000(1-1)	
Strip_43	AWT_000000(1-1)	
Strip_44	AWT_000000(1-1)	
Strip_45	AWT_000000(1-1)	
Strip_46	AWT_000000(1-1)	
Strip_47	AWT_000000(1-1)	
Strip_48	AWT_000000(1-1)	
Strip_49	AWT_000000(1-1)	
Strip_50	AWT_000000(1-1)	
Strip_51	AWT_000000(1-1)	
Strip_52	AWT_000000(1-1)	
Strip_53	AWT_000000(1-1)	
Strip_54	AWT_000000(1-1)	
Strip_55	AWT_000000(1-1)	
Strip_56	AWT_000000(1-1)	
Strip_57	AWT_000000(1-1)	
Strip_58	AWT_000000(1-1)	
Strip_59	AWT_000000(1-1)	
Strip_60	AWT_000000(1-1)	
Strip_61	AWT_000000(1-1)	
Strip_62	AWT_000000(1-1)	
Strip_63	AWT_000000(1-1)	
Strip_64	AWT_000000(1-1)	

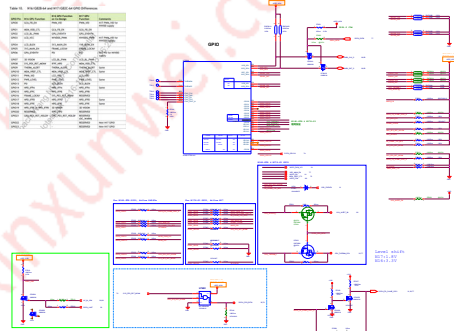
Table 5.6: SMI, ACT, AGGR, DEPR, SML, POE, CPE, VGA, DEVICE

Device	SMI	ACT	AGGR	DEPR	SML	POE	CPE	VGA	DEVICE
1	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	2
3	0	0	0	0	0	0	0	0	3
4	0	0	0	0	0	0	0	0	4
5	0	0	0	0	0	0	0	0	5
6	0	0	0	0	0	0	0	0	6
7	0	0	0	0	0	0	0	0	7
8	0	0	0	0	0	0	0	0	8
9	0	0	0	0	0	0	0	0	9
10	0	0	0	0	0	0	0	0	10
11	0	0	0	0	0	0	0	0	11
12	0	0	0	0	0	0	0	0	12
13	0	0	0	0	0	0	0	0	13
14	0	0	0	0	0	0	0	0	14
15	0	0	0	0	0	0	0	0	15
16	0	0	0	0	0	0	0	0	16
17	0	0	0	0	0	0	0	0	17
18	0	0	0	0	0	0	0	0	18
19	0	0	0	0	0	0	0	0	19
20	0	0	0	0	0	0	0	0	20
21	0	0	0	0	0	0	0	0	21
22	0	0	0	0	0	0	0	0	22
23	0	0	0	0	0	0	0	0	23
24	0	0	0	0	0	0	0	0	24
25	0	0	0	0	0	0	0	0	25
26	0	0	0	0	0	0	0	0	26
27	0	0	0	0	0	0	0	0	27
28	0	0	0	0	0	0	0	0	28
29	0	0	0	0	0	0	0	0	29
30	0	0	0	0	0	0	0	0	30
31	0	0	0	0	0	0	0	0	31
32	0	0	0	0	0	0	0	0	32
33	0	0	0	0	0	0	0	0	33
34	0	0	0	0	0	0	0	0	34
35	0	0	0	0	0	0	0	0	35
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37	0	0	0	0	0	0	0	0	37
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39	0	0	0	0	0	0	0	0	39
40	0	0	0	0	0	0	0	0	40
41	0	0	0	0	0	0	0	0	41
42	0	0	0	0	0	0	0	0	42
43	0	0	0	0	0	0	0	0	43
44	0	0	0	0	0	0	0	0	44
45	0	0	0	0	0	0	0	0	45
46	0	0	0	0	0	0	0	0	46
47	0	0	0	0	0	0	0	0	47
48	0	0	0	0	0	0	0	0	48
49	0	0	0	0	0	0	0	0	49
50	0	0	0	0	0	0	0	0	50
51	0	0	0	0	0	0	0	0	51

Group		Group/Posting Number
Group	Group/Posting Number	Group/Posting Number
1	1	1
2	2	2
3	3	3
4	4	4
5	5	5
6	6	6
7	7	7
8	8	8
9	9	9
10	10	10
11	11	11
12	12	12
13	13	13
14	14	14
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91	91	91
92	92	92
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99	99	99
100	100	100

[illegible]

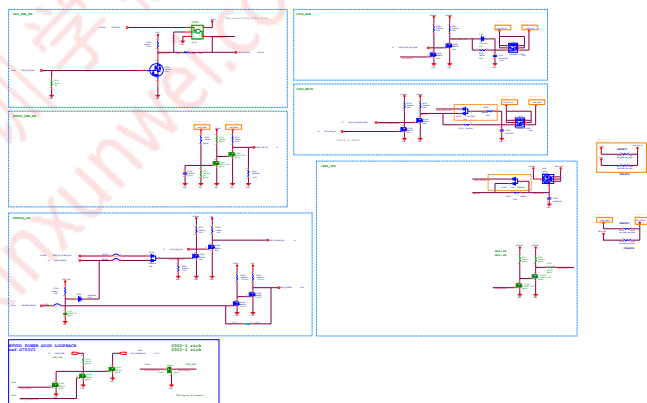
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1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
---	---	---	---	---	---	---	---	---	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	-----

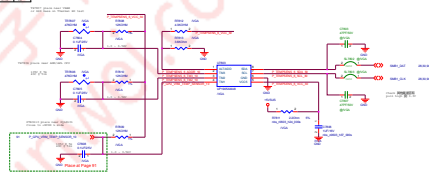
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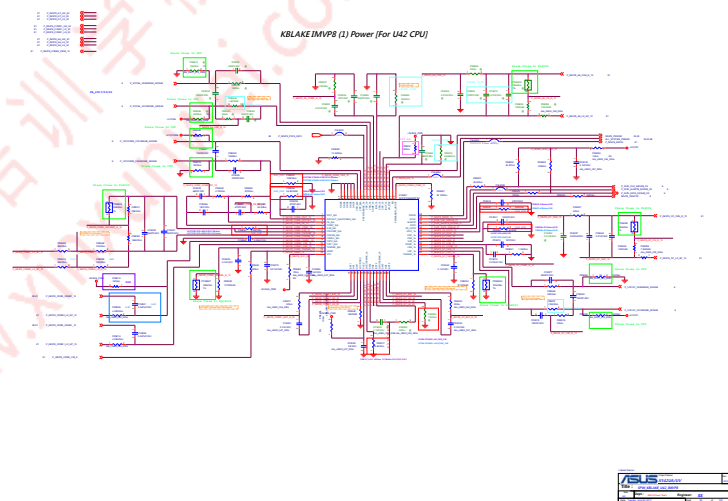
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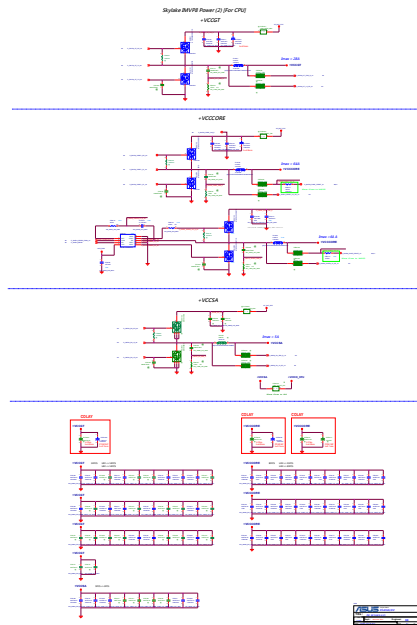


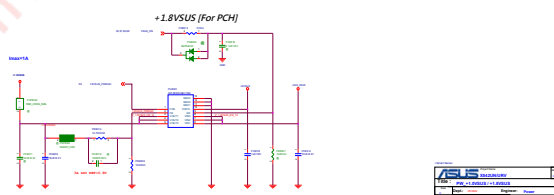
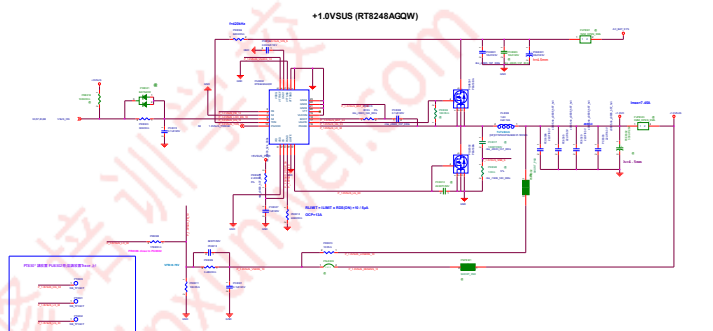
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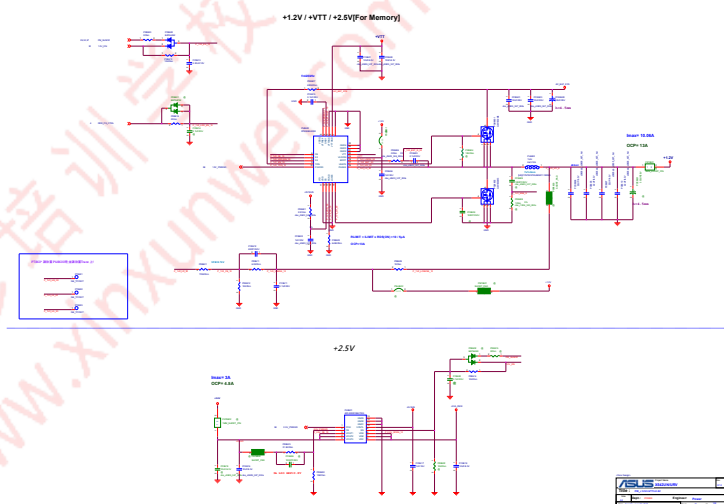


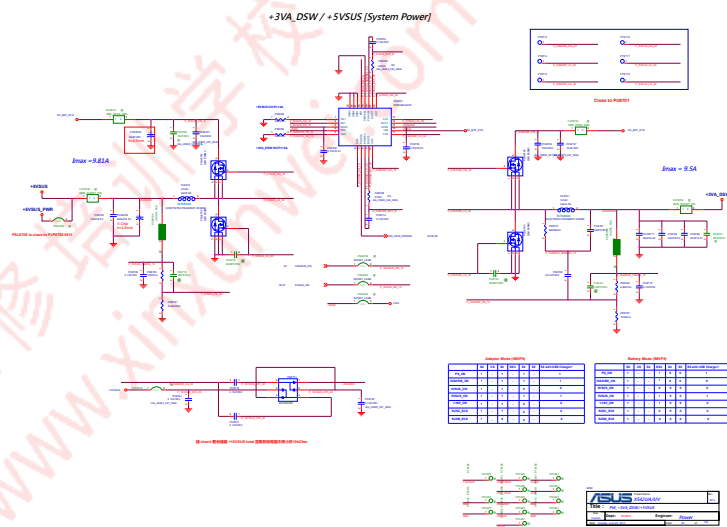


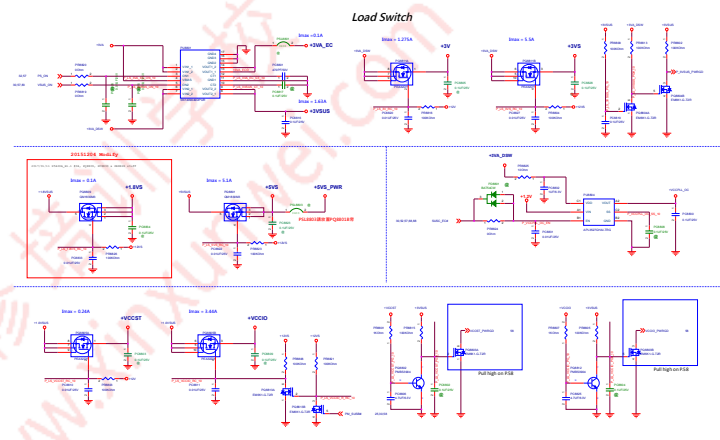










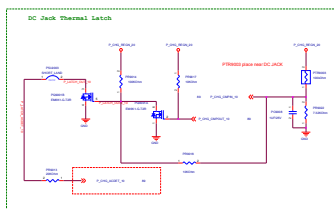
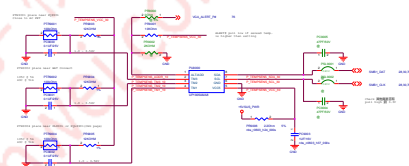


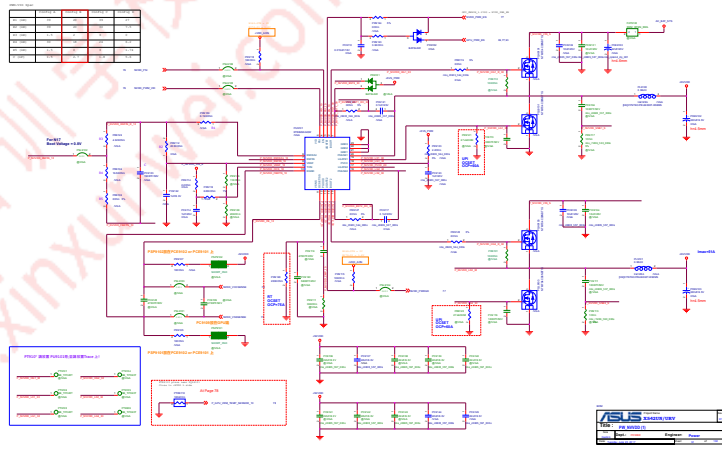
ASUS X580V10V			
PMOS SW1			
Pin	1	2	3
Signal	SW1	SW2	SW3

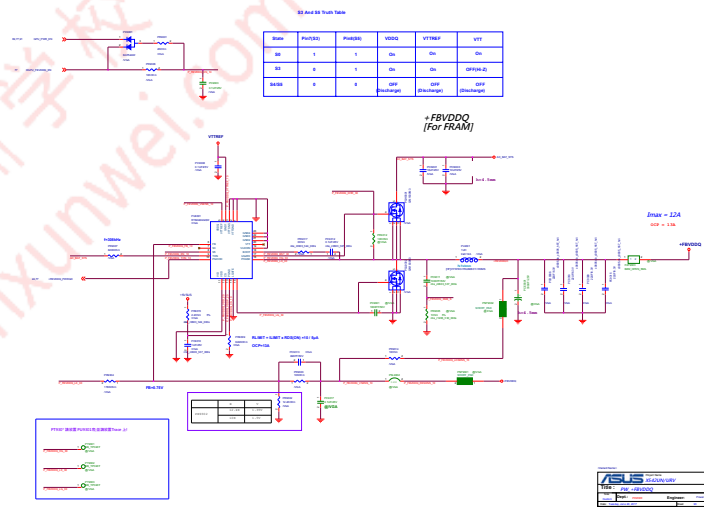


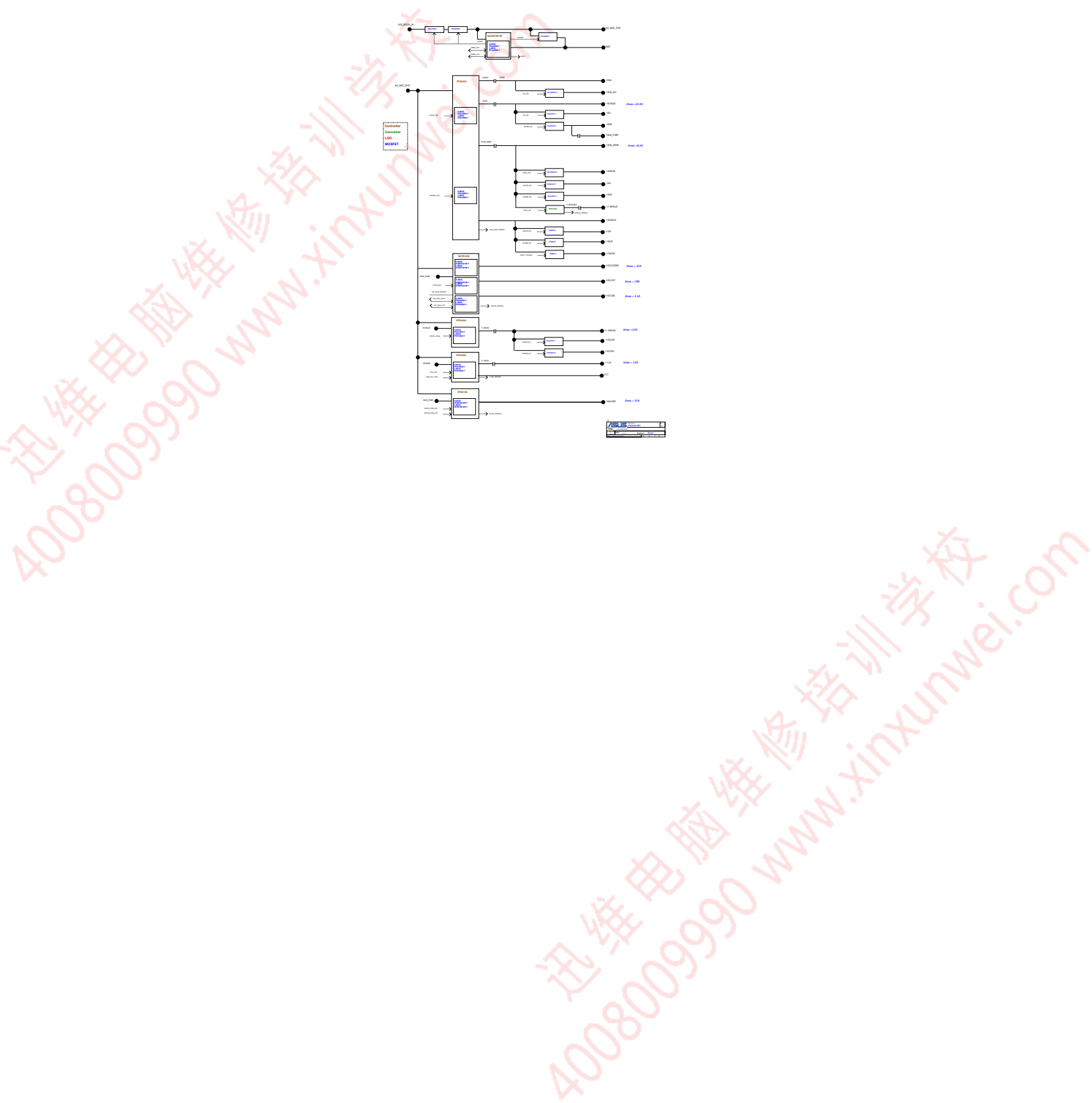
Address	Function	Value
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0x00000003	0x00000003	0x00000003
0x00000004	0x00000004	0x00000004
0x00000005	0x00000005	0x00000005
0x00000006	0x00000006	0x00000006
0x00000007	0x00000007	0x00000007
0x00000008	0x00000008	0x00000008
0x00000009	0x00000009	0x00000009
0x0000000A	0x0000000A	0x0000000A
0x0000000B	0x0000000B	0x0000000B
0x0000000C	0x0000000C	0x0000000C
0x0000000D	0x0000000D	0x0000000D
0x0000000E	0x0000000E	0x0000000E
0x0000000F	0x0000000F	0x0000000F

Register	Address	Value
0x00000000	0x00000000	0x00000000
0x00000001	0x00000001	0x00000001
0x00000002	0x00000002	0x00000002
0x00000003	0x00000003	0x00000003
0x00000004	0x00000004	0x00000004
0x00000005	0x00000005	0x00000005
0x00000006	0x00000006	0x00000006
0x00000007	0x00000007	0x00000007
0x00000008	0x00000008	0x00000008
0x00000009	0x00000009	0x00000009
0x0000000A	0x0000000A	0x0000000A
0x0000000B	0x0000000B	0x0000000B
0x0000000C	0x0000000C	0x0000000C
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0x0000000F	0x0000000F	0x0000000F



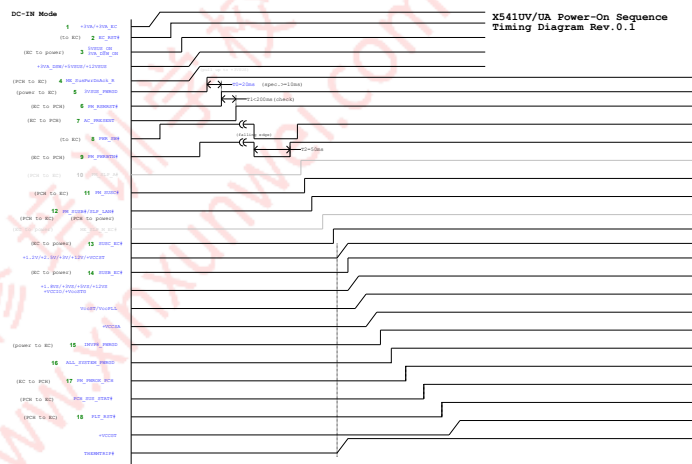












№	Имя	№	Имя
1	А.А. Абрамов	1	А.А. Абрамов
2	Б.Б. Бабич	2	Б.Б. Бабич
3	В.В. Вавилов	3	В.В. Вавилов
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6	Е.Е. Емельянов	6	Е.Е. Емельянов
7	З.З. Завьялов	7	З.З. Завьялов
8	И.И. Иванов	8	И.И. Иванов
9	К.К. Кавалер	9	К.К. Кавалер
10	Л.Л. Лавров	10	Л.Л. Лавров
11	М.М. Маврин	11	М.М. Маврин
12	Н.Н. Навои	12	Н.Н. Навои
13	О.О. Овчинников	13	О.О. Овчинников
14	П.П. Павлов	14	П.П. Павлов
15	Р.Р. Равицкий	15	Р.Р. Равицкий
16	С.С. Савицкий	16	С.С. Савицкий
17	Т.Т. Таврический	17	Т.Т. Таврический
18	У.У. Уваров	18	У.У. Уваров
19	Ф.Ф. Фаворский	19	Ф.Ф. Фаворский
20	Х.Х. Хавин	20	Х.Х. Хавин
21	Ц.Ц. Цавицкий	21	Ц.Ц. Цавицкий
22	Ч.Ч. Чавин	22	Ч.Ч. Чавин
23	Ш.Ш. Шавин	23	Ш.Ш. Шавин
24	Щ.Щ. Щавин	24	Щ.Щ. Щавин
25	Ъ.Ъ. Ъавин	25	Ъ.Ъ. Ъавин
26	Ы.Ы. Ыавин	26	Ы.Ы. Ыавин
27	Э.Э. Эванди	27	Э.Э. Эванди
28	Ю.Ю. Юванди	28	Ю.Ю. Юванди
29	Я.Я. Яванди	29	Я.Я. Яванди
30	З.З. Завьялов	30	З.З. Завьялов
31	И.И. Иванов	31	И.И. Иванов
32	К.К. Кавалер	32	К.К. Кавалер
33	Л.Л. Лавров	33	Л.Л. Лавров
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69	Ш.Ш. Шавин	69	Ш.Ш. Шавин
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